A Local Prefix Certificate and a Conditional Clock Overlap for the UD Diamond

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Codex-assisted mathematical development

20 October 2026 — Version 0.1

Abstract

We replace the full-box sensitivity estimate by a preparation-specific bound for the short CD-1 Gauss discriminator. Exact symbolic majorants give target Lipschitz constant four and actual speed bound 8/5 on an explicit box. A joint tracking/state barrier closes the use of that box. The resulting controller allocation admits a conditional physical clock interval containing 1/60 second, with a fast SAR acquisition route and catalogue LC values. This closes the timing-overlap design question under stated premises; calibration, parasitics, noise-tail qualification and actuator identification remain OPEN.

Status. DERIVED CONDITIONAL; CANDIDATE component route; development, no registry entry; constructor checks only; independent review pending; no experiment; physical promotion 0.

1 An explicit preparation box

Use CAM/CD-1's real coordinates $z = (\theta, E, x, y, u, v)$, four entries per block, and the same Hamiltonian and graph as FCAL. The three laws are nominal, entire second-species sign reversed, and electric response frozen. The initial reference is $\theta = E = y = v = 0$, $x = u = (1, 1, 1, 1)/\sqrt{2}$. Consider the convex lifted-angle box

$$D = \{|\theta_e| \le 1/100,\ |E_e|, |y_i|, |v_i| \le 1/50,\ 2/3 \le x_i, u_i \le 3/4\}. \tag{1}$$

Theorem 1 (Local majorants)**.** *On D all three laws satisfy*

$$\mathrm{Lip}_\infty(F_s) \le 8801/2500 < 4, \qquad \sup_D \|F_s\|_\infty \le 3751/2500. \tag{2}$$

The local Gauss generator has Lipschitz constant at most $177/50 < 4$.

Proof. Differentiate the explicit CD-1 Hamiltonian in real canonical coordinates. Expand each Jacobian entry into monomials; weight state factors by (1), bound cosine by one, and bound sine of each linear phase by that phase's absolute coefficient sum on D. Sum coefficient magnitudes rowwise. The largest electric row is 1716029/500000; the largest matter row is 8801/2500. The speed maximum is 3751/2500. Each Gauss row is at most $2 + 2(3/4) + 2(1/50) = 177/50$. Reversing matter signs or zeroing electric rows cannot increase these majorants. □

The accompanying symbolic program verifies every row exactly. These are conservative analytic inequalities, not trajectory samples. We adopt $L = 4$, $L_G = 4$ and actual speed $M = 8/5$ below.

2 Closing the local and tracking assumptions

Assume preparation error $e_0 = 1/10000$, endpoint reconstruction error $m = 1/10000$, input error $\nu = 3/100000$, and continuous field defect at most $\delta = 1/100$. Put $h_\pm = 1/100 \pm 1/100000$. Under the SAC controller model with plant Lipschitz bound $\lambda \le 1$, the command $U_s = F_s - F_0$ has bound $K_U \le 5$ on D.

Theorem 2 (Prefix closure and robust decisions)**.** *Suppose prehistory lies in the same box with speed at most* $8/5$*, reconstructed prehistory arguments lie in* D*, all sample ages and numerical errors obey the specified budgets, and the static residual is* $p \le 3/400$*. If the initial tracking mismatch and the actuator's steady tracking bound are both strictly below* $\rho = 1/400$*, then the local state/speed assumptions close through* h_+*. Both controller arguments and reconstructed decision endpoints remain in* D*.*

Proof. Until a first exit from the state/reconstruction box or tracking barrier, the field defect is at most $p + \rho = 1/100$. Therefore actual speed is at most $3751/2500 + 1/100 < 8/5$. SAC's tracking inequality with this speed keeps error strictly below ρ, excluding the tracking exit.

For all non-angle coordinates, displacement from the reference preparation, including the larger reconstruction radius, is at most

$$d_* = e_0 + (8/5)h_+ + \max(m, \nu) = 0.016216.$$

Use $7/10 < 1/\sqrt{2} < 71/100$ to check the large-coordinate bounds in (1); the small-coordinate margin is $0.02 - d_* = 0.003784 > 0$. For angles, use $\theta'_e = E_e$ in each ideal law and charge the actual defect: $|\theta_e| \le e_0 + (1/50 + \delta)h_+ + \max(m, \nu) < 1/100$. Thus a first state exit is also impossible. The prehistory and release premises remain actual instrument requirements; bounded hold radius alone does not establish speed. □

The perturbation and certified Gauss-decision errors sharpen to

$$\eta = \frac{e_0 + \delta h_+}{1 - 4h_+} = \frac{2001}{9599600}, \qquad B = 4(\eta + e_0) + 16m = \frac{8501}{2999875}. \tag{3}$$

The $16m$ includes both observed endpoint uncertainty and the additional certified decision-interval radius. Retaining FCAL's exact ideal fault bounds $q_w(h) = 2h - 8h^2 - 11h^3/8$ and $q_f(h) = 2h - 8h^3/3$, the nominal/fault slacks against $T(h) = (1 + h)/100$ are approximately:

Nominal passage	0.00726611526
Wrong-species-sign detection	0.00624634358
Frozen-electric detection	0.00704345658

The initial certified Gauss upper bound is $4e_0 + 8m = 0.0012 < 0.01$. This theorem concerns only the stated short preparation prefix.

3 A conditional clock interval with series resistance

Include measured series loss in the physical plant:

$$\dot{\Phi} = Q/C - (R/L)\Phi + V, \qquad \dot{Q} = -\Phi/L + I. \tag{4}$$

Balanced common-action scales give $\alpha = \beta = t_0/\sqrt{LC}$ and $\gamma = Rt_0/L$. The normalized plant has $F_0(X, Y) = (-\gamma X + \beta Y, -\alpha X)$ and $\lambda \le \gamma + \alpha$. The active commands cancel the retained loss term as well as the reactive plant; unmodeled loss remains in p.

As a *conditional catalogue-corner screen*, require actual operating-band bounds

$$L \ge 17/20 \text{ H}, \quad C \ge 1/1250 \text{ F}, \quad R \le 529/80\ \Omega. \tag{5}$$

Then $R/L < 8\ \text{s}^{-1}$ and $1/\sqrt{LC} < 40\ \text{s}^{-1}$, so $\lambda < 48t_0$ and $\lambda \le 1$ is guaranteed when $t_0 \le 1/48$ s.

Propose a 1 μs command-update period, at most 2 μs additional true sensing-to-command latency, and an identified actuator time constant at most 1 μs. Thus age plus actuator time constant is at most 4 μs. With $\nu = 3/100000$, $q = 1/25000$ and $\epsilon_a = 1/100000$, SAC's local tracking bound is

$$b(t_0) \le \frac{8(4\,\mu\text{s})}{t_0} + 5\nu + q + \epsilon_a. \tag{6}$$

The sufficient tracking allocation $b < 1/400$ therefore gives the nonempty interval

$$\boxed{8/575 < t_0 \le 1/48 \text{ s}}. \tag{7}$$

At $t_0 = 1/60$ s, $b = 53/25000$ and total residual is

$$p + \max(\sigma, b) = \frac{481}{50000} = 0.00962 < 0.01, \qquad \sigma \le 1/1000. \tag{8}$$

The slack is 19/50000. The 1/100 prefix lasts 1/6000 s, approximately 166.667 μs. This interval replaces neither CPC's full-box allocation nor its exact LC identity; it uses a smaller, proved preparation region and a different timing budget.

A concrete source-screened route

Hammond 193S is listed as 1 H, 5.75 Ω, with series tolerances of 15%; inductance is specified at rated DC current [1]. Nichicon UES1C102MHM is a bipolar 1000 μF capacitor with 20% tolerance at the catalogue measurement conditions [2]. These motivate (5), but do not prove it at the small operating bias or over the transient spectrum. Inductor hysteresis, capacitance dispersion, ESR, leakage, temperature and actual loading need measurement.

Nominal common scales can use $Q_0 = 10^{-4}$ C and $\Phi_0 = \sqrt{10}/1000$ Wb. Then $S_{\text{action}} = \sqrt{10}/10^7$ J s. Actual channel scales must be rebalanced after calibration while retaining a common action; nominal values cannot simply be reused across unequal components.

4 Converter, startup and noise gates

AD4630-24 supports two simultaneous 24-bit channels at a listed maximum 2 MSPS; its conversion-time maximum is 300 ns under the specified conditions [3]. It is a candidate for unaveraged acquisition. The AD5791 uses a 24-bit write word and up to 35 MHz serial clock [4]. A frame needs at least $24/(35\,\mathrm{MHz})$, so fresh 2 MHz writes are not supported by that interface. The proposed command rate is 1 MHz; the complete 2 μs latency still needs timing closure over all channels. DAC settling entries do not establish the required first-order model.

The controller needs 24 state coordinates (twelve dual-channel ADC devices for fully parallel acquisition); additional independent coupling witnesses and actuator/work sensing remain required. Parallel transfers, timestamp skew, code evaluation, lookup error, synchronization and command latching are part of the latency/error budget. No complete FPGA or analog-driver design has been admitted.

A conditional preload rule

On D, $\|U_s\|_\infty \le 3751/2500 + 3/4 < 5/2$. Starting the actuator at zero and holding the state within $r_h = 1/20000$ of a fixed center, with every used history in that tube, a ten-time-constant preload gives

$$\|a - U_s(z_0)\|_\infty < \frac{5/2}{20000} + 5(2r_h + \nu) + q + \epsilon_a = \frac{33}{40000} < \frac{1}{1000}. \tag{9}$$

The exact positive Taylor bound $e^{10} > 20000$ is inherited from SAC. With the proposed time constant this preload lasts at least 10 μs. Hold work, release kicks and prehistory speed require separate records.

A noise-family certificate, only with a tail premise

Suppose at most $N = 10000$ controller-coordinate errors enter the prefix decision, deterministic error is at most 6 ppm, and every random error has two-sided sub-Gaussian scale at most 4 ppm. Then a 24-ppm noise allowance gives

$$\Pr(\text{any input error} > 30 \text{ ppm}) \le 2Ne^{-18} < 1/500. \tag{10}$$

No independence is needed. The calculator proves $e^{18} > 10^7$ by a positive Taylor partial sum. Supplier RMS/SNR figures do not establish the tail premise. Calibration uncertainty, witness readout, clocks, endpoints and the rest of the run need their own joint failure allocation; this input-family bound is not whole-campaign coverage.

Why hardware remains HOLD

The capacitor's listed leakage limit is 480 μA under its rated-voltage test [2]. At the nominal scales above, the entire $p = 3/400$ allowance corresponds to only 45 μA in a charge-current port, before other errors. The catalogue limit cannot certify that budget; neither can it predict leakage at the much smaller test voltage. A measured charge/voltage/leakage map or bounded compensation is required. ESR and dielectric memory also require a valid retained-state map.

The next return must substantiate operating-band L, C, R, canonical readout, input tails and gain/offset drift, full latency, actual actuator residual, range/slew, leakage/parasitics, startup and independent witnesses. No parts were purchased and no experiment was executed.

5 Reproducibility, provenance and scope

`verify_prefix_box.py` checks all local Hamiltonian Jacobian, speed and Gauss majorants in exact symbolic arithmetic, including both fault laws. `prefix_feasibility_certificate.py` checks twelve exact arithmetic controls: clock interval, residual and barrier margins, startup, negative clocks, catalogue-corner inequalities, preparation anchors, a conditional noise union bound and serial-frame timing. Exact calculations are constructor checks, not independent review.

Dependencies are CAM/CD-1, FCAL, SAC and CPC v0.1. The Hamiltonian, fault definitions and engineering Gauss gate are unchanged. This manuscript re-derives the local constants against the explicit source model and does not improve physical status by citing conditional results. No full-horizon CD-1 or SDW admission, autonomous hardware Hamiltonian, or grand-unification correspondence is asserted.

Primary manufacturer sources

Accessed during the 20 October 2026 Chicago work session (21 October UTC).

1. Hammond Manufacturing, *193 Series DC Filter Chokes*, 193S row and measurement conditions. Manufacturer specification.

2. Nichicon, *UES1C102MHM* and UES series data sheet, catalogue measurement conditions. Part specification. Series data sheet.

3. Analog Devices, *AD4630-24/AD4632-24*, Rev. B, specifications and transfer timing. Manufacturer data sheet.

4. Analog Devices, *AD5791*, Rev. F, serial interface and conditional settling specifications. Manufacturer data sheet.

The circuit values are a source-screened candidate route. Supplier tolerances, catalogue test frequencies and bias conditions are not automatically operating-band guarantees. Identification data and non-constructor adversarial review remain OPEN.

Claim footer. DERIVED CONDITIONAL mathematics; CANDIDATE clock-compatible route; hardware HOLD; development, no registry entry; constructor verification only; independent review pending; empirical execution NONE; physical promotion 0.